REMARKS

Claims 1-36 are pending in the present application. Claims 4, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, and 29-36 are withdrawn. By virtue of this response, claims 1, 6, 10, 18, and 22 have been amended, without prejudice or disclaimer of any previously claimed subject matter. Accordingly, claims 1-3, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, and 28 are currently under consideration. Amendment of certain claims is not to be construed as a dedication to the public of any of the subject matter of the claims as previously presented. Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attachment is entitled "**VERSION WITH MARKINGS TO SHOW CHANGES MADE.**"

Allowable Subject Matter

Claims 10, 12, 16, 18, 20, and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claim 10 (from which claims 12 and 16 depend) and claim 18 (from which claims 20 and 26 depend) have been amended into independent form. Accordingly, Applicants submit that claims 10, 12, 16, 18, 20, and 26 are in condition for allowance.

Title

The Examiner contends that the title of the invention is not descriptive. Accordingly, the title is amended as indicated above.

Abstract

The Examiner objects to the abstract due to informalities. The abstract has been amended as indicated above to obviate this objection.

Drawings

The Examiner objects to Figures 22 and 23 because they "should be designated by a legend such as --Prior Art--." Accordingly, submitted herewith is an amendment to the Drawings. In particular, Figures 22 and 23 are designated by the legend "Prior Art."

Rejections under 35 U.S.C. §112, First Paragraph

Claims 22, 24, and 28 are rejected under 35 U.S.C. § 112, first paragraph. Specifically, the Examiner states that the specification "never discloses the drain terminals ... are connected to each other to from an output terminal as claimed in claim 22." In the amendment herein, in Claim 22, "drain terminals" is replaced by "source terminals." Support for the amendment is found in the present application, for example, on page 35, lines 6-17 and Figure 16. The Applicants therefore request withdrawal of the rejection.

Rejections under 35 U.S.C. § 102(e)

Claims 1-3 stand rejected under 35 U.S.C. § 102(e) as allegedly anticipated by Merrill et al., U.S. Patent No. 5,786,617 (hereinafter "Merrill").

Claim 1 is amended to recite, in part, "said well in each of said semiconductor elements is provided with a substrate which receives a second input signal through a contact hole formed therein at a region other than said source region and drain region." Support for the amendment is found in the present application, for example, at page 16, lines 2-22.

The Examiner states, *inter alia*, that Merrill shows "a substrate terminal through a contact hole formed therein at a region [38a, 48a] other than the source region and drain region." The contact region 38a of Merrill, however, is connected to a fixed "low voltage V_{dd}, e.g., 3.3 volts." (Merrill: col. 4, lines 27-30). The region 48a is "connected to Vss which is ground (0 volts)." (Merrill: col. 4, lines 31-39). The regions 38a and 48a of Merrill receive only fixed voltages and are therefore not "a substrate which receives a second input signal," as recited in amended claim

1. As described in the specification of the present application at page 16, lines 16-22, the first input terminal and the second input terminal "receive inputs IN1 and IN2, which are different signals synchronized to each other based on a clock signal or the like." Accordingly, the "second input signal," received by the substrate is not a fixed voltage. Therefore, Merrill does not disclose or suggest the limitations of amended claim 1, specifically, "a substrate which receives a second input signal."

The Applicants therefore request withdrawal of the rejection.

Rejections under 35 U.S.C. §103(a)

Claims 1-3 stand rejected under 35 U.S.C. §103(a) as allegedly obvious over Chang et al., U.S. Patent No. 3,865,654 (hereinafter "Chang").

As stated above, claim 1 is amended to recite, in part, "said well in each of said semiconductor elements is provided with a substrate which receives a second input signal through a contact hole formed therein at a region other than said source region and drain region." Support for the amendment is found in the present application, for example, at page 16, lines 2-22.

The Examiner states, *inter alia*, that Chang discloses "a substrate terminal contact hole formed therein at a region [28,30] other than the source region and drain region." Chang, however, merely discloses that region 28 is a P-pocket contact region (Chang: col. 5, lines 45-52) and that region 30 is an N-type diffusion (Chang: col. 6, lines 16-17). The regions 28 and 30 are clearly not substrate regions that receive an "input signal through a contact hole" as recited in claim 1. Furthermore, Chang does not disclose or suggest applying an input signal to the regions 28 and 30. As described in the specification of the present application on page 16, lines 16-22, the first input terminal and the second input terminal "receive inputs IN1 and IN2, which are different signals synchronized to each other based on a clock signal or the like." Therefore, Change does not disclose or suggest all of the limitations of claim 1.

There would have been no motivation from Chang to make the devices having the features recited in the claims. The Applicants therefore request withdrawal of the rejection.

Claims 6, 8, and 14 stand rejected under 35 U.S.C. §103(a) as allegedly obvious over over Chang in view of Iwamatsu, Japanese Patent Publication No. 07-078885 (hereinafter "Iwamatsu").

Claims 6, 8, and 14 depend from claim 1. As discussed above, Chang fails to teach all of the limitations of claim 1. Specifically, Chang fails to disclose or suggest the claimed semiconductor device, wherein "said well in each of said semiconductor elements is provided with a substrate which receives a second input signal through a contact hole formed therein at a region other than said source region and drain region," as recited in claim 1. Chang merely discloses that region 28 is a P-pocket contact region (Chang: col. 5, lines 45-52) and that region 30 is an N-type diffusion (Chang: col. 5, lines 16-17). The regions 28 and 30 are clearly not substrate regions that receive an "input signal through a contact hole" as recited in claim 1. Furthermore, Chang does not disclose or suggest applying an input signal to the regions 28 and 30. Therefore, Change does not disclose or suggest all of the limitations of claim 1.

The deficiencies of Chang are not met by the addition of Iwamatsu. Further, there is no motivation from the art applied by the Examiner to select a semiconductor device having the features of the recited claims.

The Applicants therefore request withdrawal of the rejection.

CONCLUSION

Applicant has, by way of the amendments and remarks presented herein, made a sincere effort to overcome rejections and address all issues that were raised in the outstanding Office Action. Accordingly, reconsideration and allowance of the pending claims are respectfully requested. If it is determined that a telephone conversation would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

In the unlikely event that the transmittal letter is separated from this document and the Patent Office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Assistant Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing docket no. 247322001700. However, the Assistant Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Dated: July 10, 2002

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Title:

The Title has been amended as follows:

FOUR TERMINAL SEMICONDUCTOR DEVICE AND DRIVING METHOD THEREOF

In the Claims:

Claims 1, 6, 10, 18, and 22 have been amended as follows.

1. (Amended) A semiconductor device comprising a plurality of semiconductor elements, each being provided with a source region having a source terminal and a drain region having a drain terminal in a well formed in a semiconductor layer, and a gate terminal fabricated on a channel region, formed between said source region and drain region, which receives a first input signal through a gate insulating film, wherein:

each of said semiconductor elements is electrically separated from the others; and

said well in each of said semiconductor elements is provided with a substrate which receives a second input signal ~~terminal~~ through a contact hole formed therein at a region other than said source region and drain region.

6. (Amended) The semiconductor device of Claim 1, wherein:

each of said semiconductor elements is composed of a pair of a P-type semiconductor element and an N-type semiconductor element;

a high potential is supplied to a source terminal of said P-type semiconductor element and a low potential is supplied to a source terminal of said N-type semiconductor element;

gate terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form ~~a~~ the first input terminal;

substrate terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form ~~a~~ the second input terminal; and

drain terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form an output terminal.

10. (Amended) A ~~The~~ semiconductor device ~~of Claim 1,~~comprising a plurality of semiconductor elements, each being provided with a source region having a source terminal and a drain region having a drain terminal in a well formed in a semiconductor layer, and a gate terminal fabricated on a channel region, formed between said source region and drain region, through a gate insulating film, wherein:

each of said semiconductor elements is electrically separated from the others;

said well in each of said semiconductor elements is provided with a substrate terminal through a contact hole formed therein at a region other than said source region and drain region;

each of said semiconductor elements is composed of a pair of a P-type semiconductor element and an N-type semiconductor element;

a high potential is supplied to a source terminal of said P-type semiconductor element and a low potential is supplied to a source terminal of said N-type semiconductor element;

a gate terminal of said P-type semiconductor element and a substrate terminal of said N-type semiconductor element are connected to each other, thereby to form a first input terminal;

a gate terminal of said N-type semiconductor element and a substrate terminal of said P-type semiconductor element are connected to each other, thereby to form a second input terminal; and

drain terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form an output terminal.

18. (Amended) A ~~The~~ semiconductor device ~~of Claim 1~~, comprising a plurality of semiconductor elements, each being provided with a source region having a source terminal and a drain region having a drain terminal in a well formed in a semiconductor layer, and a gate terminal fabricated on a channel region, formed between said source region and drain region, through a gate insulating film, wherein:

each of said semiconductor elements is electrically separated from the others;

said well in each of said semiconductor elements is provided with a substrate terminal through a contact hole formed therein at a region other than said source region and drain region;

each of said semiconductor elements is composed of a pair of a P-type semiconductor element and an N-type semiconductor element;

a drain terminal of said N-type semiconductor element is supplied with a high potential and a drain terminal of said P-type semiconductor element is supplied with a low potential;

gate terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form a first input terminal;

substrate terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form a second input terminal; and

source terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form an output terminal.

22. (Amended) The semiconductor device of Claim 1, wherein:

each of said semiconductor elements is composed of a P-type semiconductor element and an N-type semiconductor element;

a high potential is supplied to a drain terminal of said N-type semiconductor element and a low potential is supplied to a drain terminal of said P-type semiconductor element;

a gate terminal of said N-type semiconductor element and a substrate terminal of said P-type semiconductor element are connected to each other, thereby to form ~~a~~ the first input terminal;

a gate terminal of said P-type semiconductor element and a substrate terminal of said N-type semiconductor element are connected to each other, thereby to form ~~a~~ the second input terminal; and

~~drain~~ source terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form an output terminal.

In the Abstract:

The Abstract on page 67 has been amended as follows:

In a semiconductor element (1) provided with a source region (3) and a drain region (4) both formed in a well (2), and a gate electrode (7) fabricated on a channel region (5), formed between these regions, through a gate insulting film ~~(8)~~ (6), each element is electrically isolated by means of an SOI substrate and a field oxide film, for example, and a substrate terminal (TW) is pulled out from the channel region (5) via a contact hole formed through an inter-layer insulating film in each element at a region other than the source region (3) and drain region (4). Consequently, a 2-input-1-output element having the gate terminal (TG) and substrate terminal (TW) as two inputs can be realized, thereby making it possible to improve a packing density and operating rate while reducing the costs when forming a logic circuit or the like.